150V N-Ch Power MOSFET

Feature

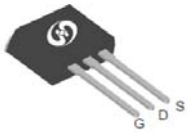
- ◇ High Speed Power Smooth Switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free

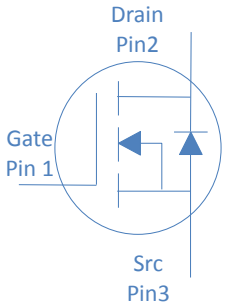
V_{DS}	150	V
$R_{DS(on),typ}$	9	mΩ
$I_{D\ (Sillicon\ Limited)}$	9	mΩ
$I_{D\ (Package\ Limited)}$	120	A
$I_{D\ (Package\ Limited)}$	120	A

Application

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ Power Tools
- ◇ UPS
- ◇ Motor Control

TO-262





Part Number	Package	Marking
HGW105N15SL	TO-262	W105N15SL

Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	120	A
		T_C=100℃	85	
Continuous Drain Current (Package Limited)		T_C=25℃	120	
Drain to Source Voltage	V_{DS}	-	150	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	400	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.4mH, T_C=25℃	500	mJ
Power Dissipation	P_D	T_C=25℃	333	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to175	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\Theta JC}$	0.45	℃/W
Thermal Resistance Junction-Ambient	$R_{\Theta JA}$	60	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	150	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1	1.9	3	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=150V, T_j=25℃	-	-	1	μA
		V_{GS}=0V, V_{DS}=150V, T_j=100℃	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	9	10.5	mΩ
		V_{GS}=10V, I_D=4.5A	-	9.8	12.5	
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	80	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	0.7	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=75V, f=1MHz	-	4059	-	pF
Output Capacitance	C_{oss}		-	302	-	
Reverse Transfer Capacitance	C_{rss}		-	11	-	
Total Gate Charge	Q_g (10V)	V_{DD}=75V, I_D=20A, V_{GS}=10V	-	57	-	nC
Total Gate Charge	Q_g (4.5V)		-	26	-	
Gate to Source Charge	Q_{gs}		-	12	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	10	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=75V, I_D=20A, V_{GS}=10V, R_G=10Ω,	-	20	-	ns
Rise time	t_r		-	10	-	
Turn off Delay Time	$t_{d(off)}$		-	32	-	
Fall Time	t_f		-	12	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=75V, I_F=20A, dI_F/dt=100A/μs	-	95	-	ns
Reverse Recovery Charge	Q_{rr}		-	285	-	nC

Fig 1. Typical Output Characteristics

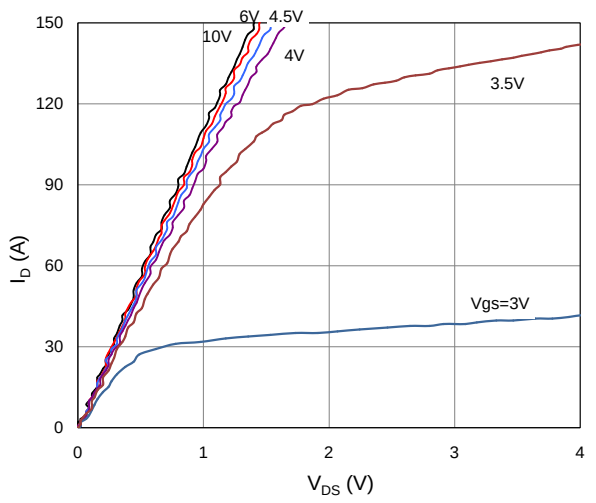


Figure 2. On-Resistance vs. Gate-Source Voltage

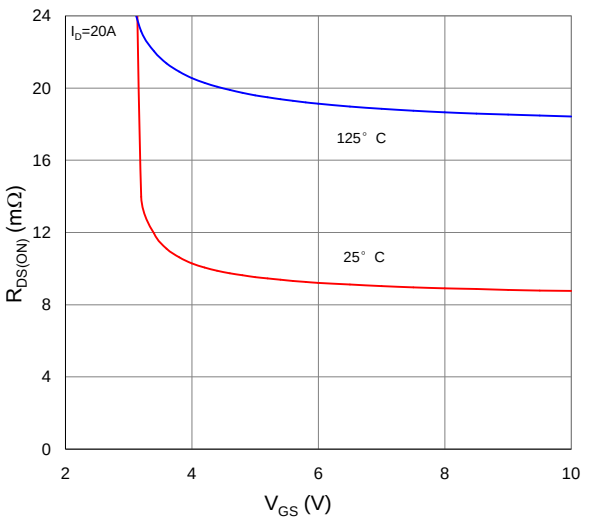


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

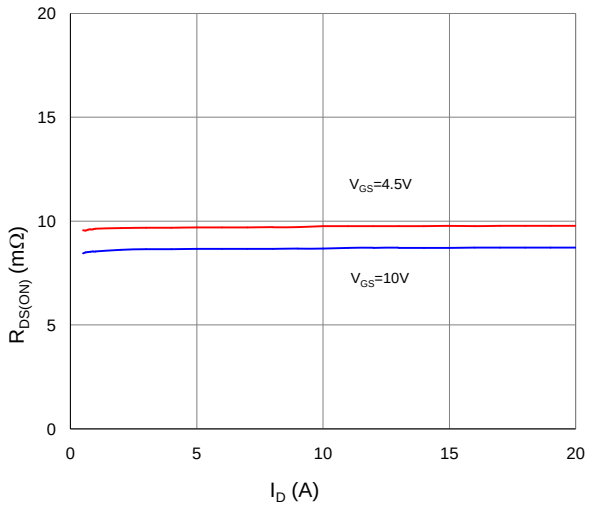


Figure 4. Normalized On-Resistance vs. Junction Temperature

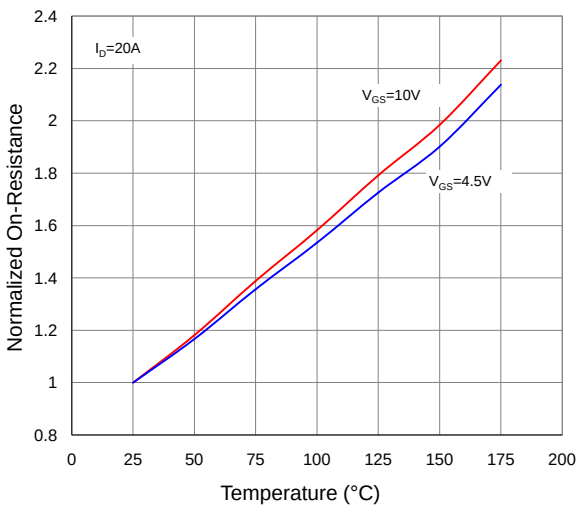


Figure 5. Typical Transfer Characteristics

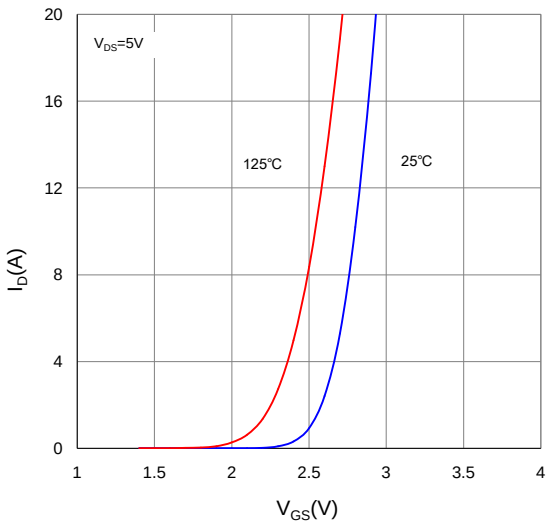


Figure 6. Typical Source-Drain Diode Forward Voltage

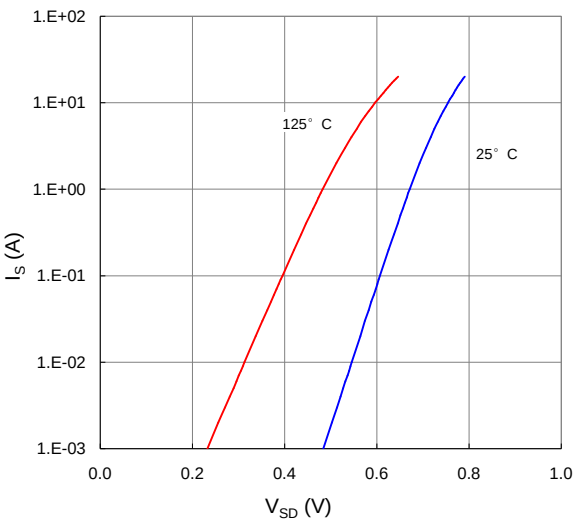


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

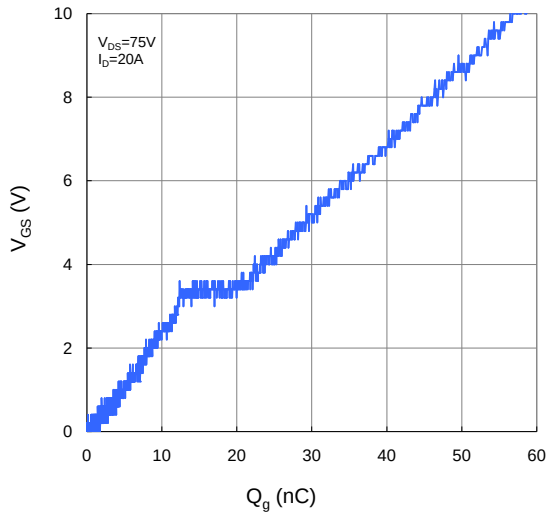


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

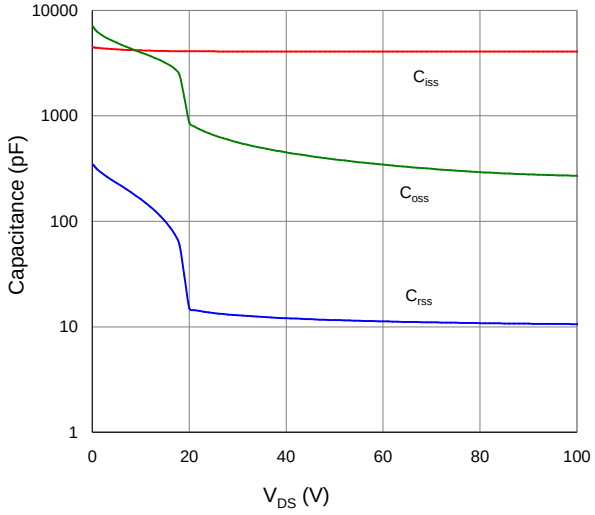


Figure 9. Maximum Safe Operating Area

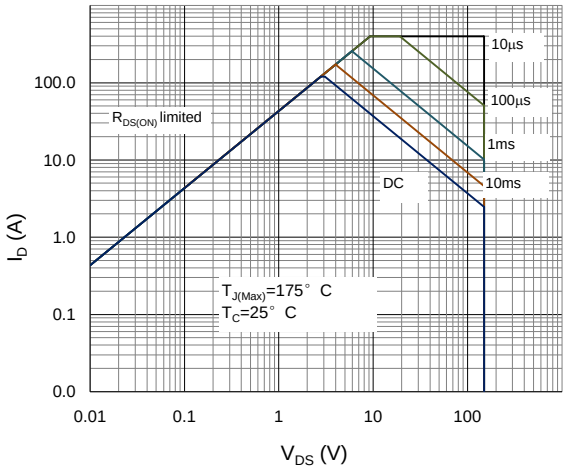


Figure 10. Maximun Drain Current vs. Case Temperature

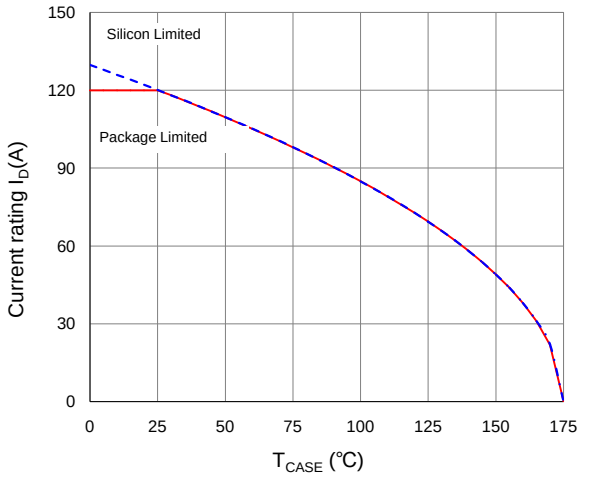
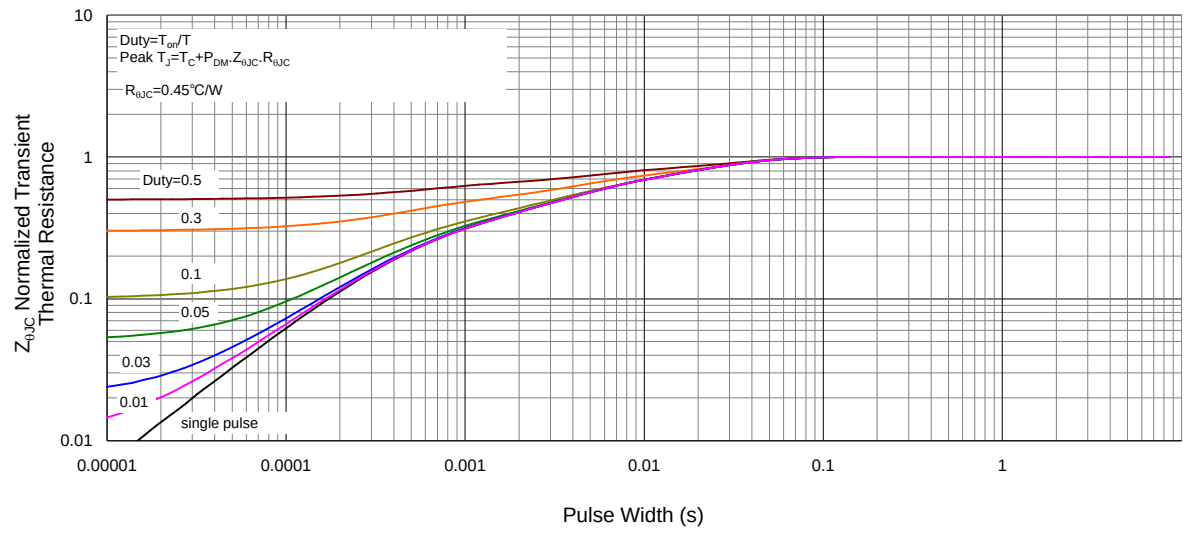
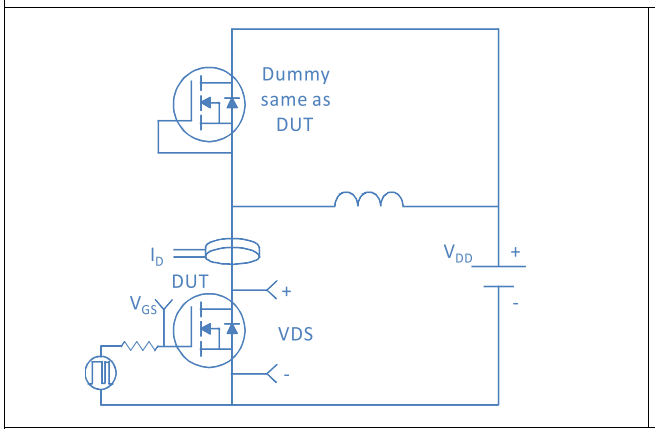
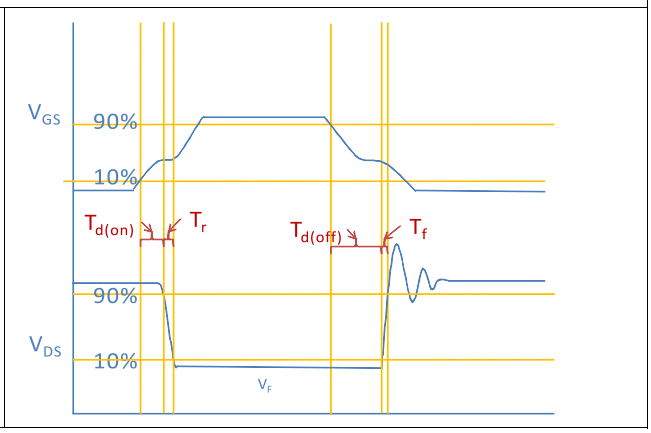


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case

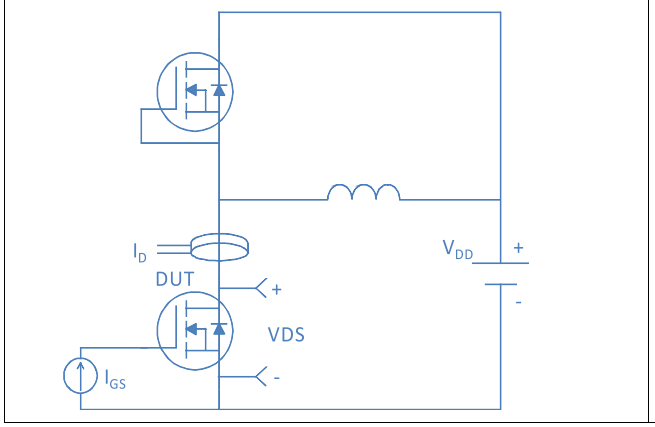


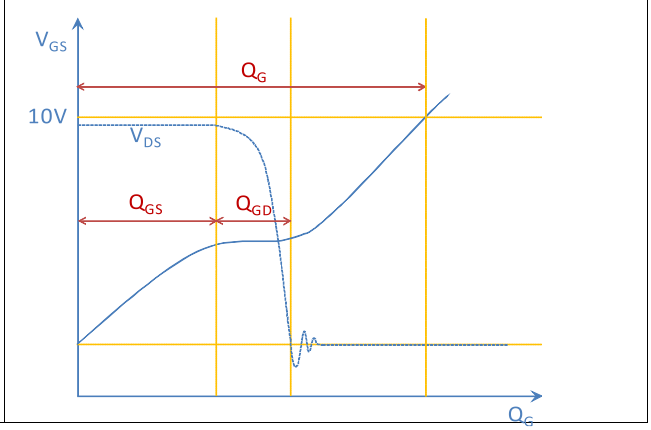
Inductive switching Test



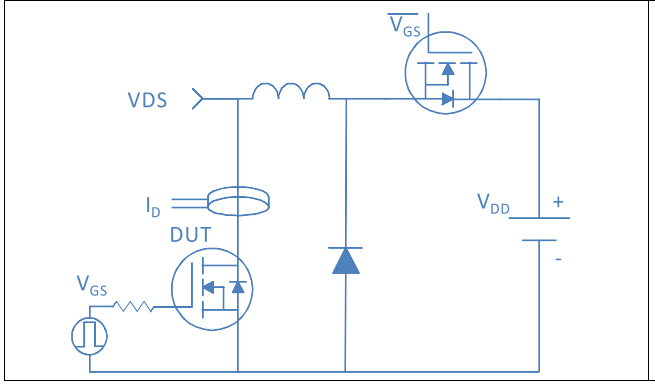


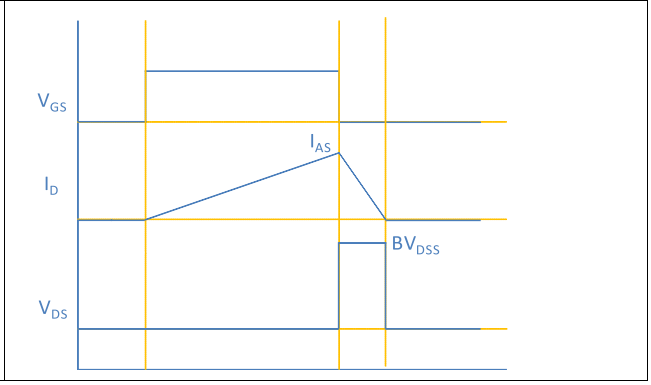
Gate Charge Test



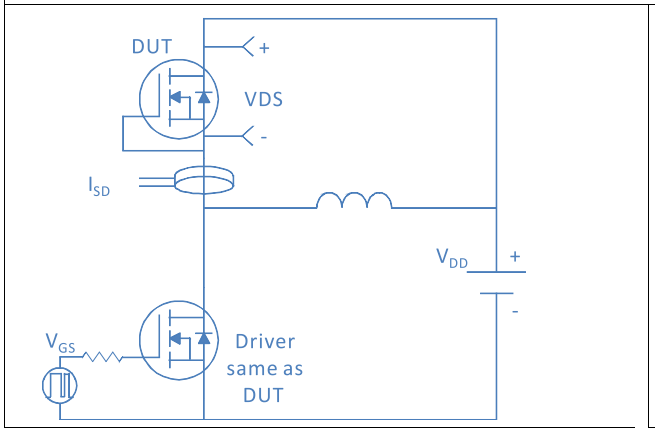


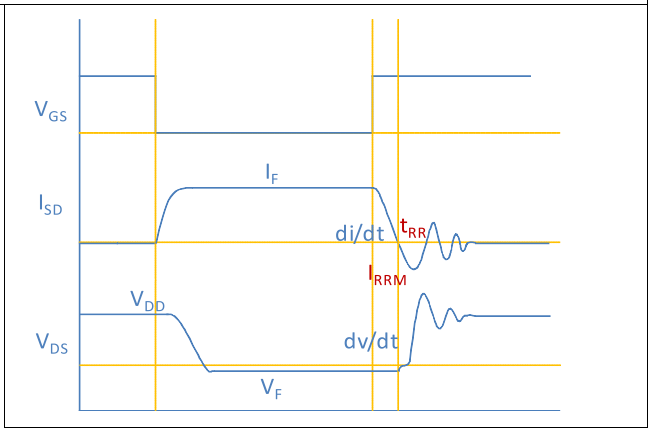
Uclamped Inductive Switching (UIS) Test



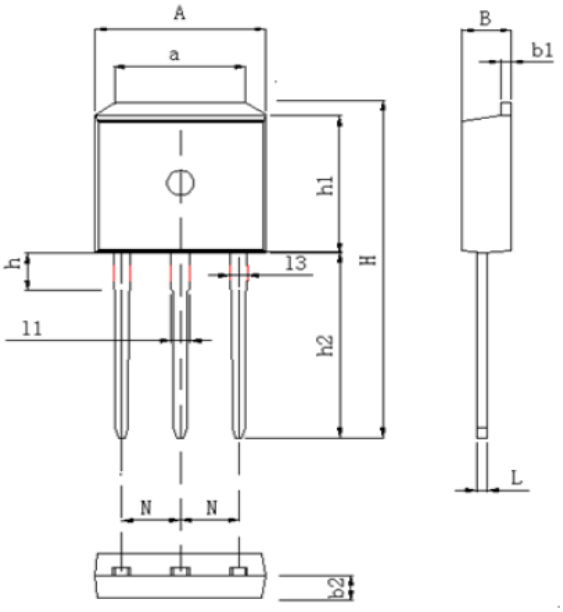


Diode Recovery Test





TO-262, 3 leads



Unit: mm

DIM	MILLIMETERS
A	9.98±0.2
a	7.4±0.4
B	4.5±0.2
b1	1.3±0.05
b2	2.4±0.2
H	23.9±0.3
h	3.1±0.2
h1	9.16±0.2
h2	13.2±0.2
L	0.5±0.1
l1	1.3±0.1
l2	0.8±0.1
N	2.45±0.1